UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,343	12/12/2003	Jerome Cornet	ALC 3108	7458

7590 09/29/2006

KRAMER & AMADO, P.C.
Suite 240
1725 Duke Street
Alexandria, VA 22314

EXAMINER	
COLEMAN, ERIC	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 09/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/733,343	CORNET ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5,6,8,10* is/are allowed.

6)☒ Claim(s) *1-4,7,9 and 11-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4,7,9,11,13,14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Desai (patent No. 6,288,656) in view of Gregg (patent No. 5,003,588) and Oh etal. (patent No. 6,959,297).

3. Desai taught the invention substantially as claimed including a data processing ("DP") system comprising (as per claims 1,13):

A) A flip-flop(704) for receiving a n bit wide stream(RXD1,RXD2 serial data)(e.g., see fig. 7 and col. 5, lines 33-59) and a corresponding first clock signal at a first rate(recovered clock)(e.g., see fig. 7), and outputting a data stream as a W times N-bit wide data stream and a corresponding stream and a corresponding second clock signal at a second rate divided by W(e.g., see col. 5, lines 33-65);

B) A bus splitter for splitting the W times N-bit wide data stream into W data streams of width N(e.g. see col. 5, lines 33-65)[the data stream is divided or split into data streams sent over plural parallel channels];

C) A plurality (W) of flip-flops (712), each flop-flop for storing data obtained by processing the pattern and for receiving a respective one of the data streams of width N as an address and the second clock signal as a clock, and each flip-flop being operable

to output a portion of the data on an M-bit wide output bus [bus comprises the output lines of the flip flops 712 for the channels e.g. see fig.7];

D) A processor (714)for receiving the portions of data on each M-bit wide output bus as data and the second clock signal as a clock, and being operable to determine whether the pattern is in the data stream in dependence upon the received portions of data and the received clock, and for outputting a pattern match signal indicating detection of the pattern in the data stream(e.g., see fig. 7 and col. 6, lines 3-21) .

4. Desai did not expressly detail (claim 1,13) the using a FIFO instead of a flip-flop for receiving the bit stream. Gregg however taught an input FIFO for receiving a data stream (e.g., see col. 2, lines 33-56).

5. It would have bee obvious to one of ordinary skill in the DP art to combine the teachings of Desai and Gregg. Both references were directed to the problems of receiving data and synchronizing the data transfer between devices and serializing and deserializing the data(e.g., see col.3, lines 20-65 of Gregg; and col. 7, lines 55-64 and col. 5, lines 46-59 of Desai). One of ordinary skill would have been motivated to incorporate the FIFO for receiving the data stream to aid in synchronizing the data transfers especially when the data link has period of idleness (e.g., see col. 2, lines 33-64).

6. Desai did not expressly detail that the data pattern after processing was stored in a RAM. Oh however taught the data pattern after processing (input processing in element 22 for putting the data in the form for comparison to be stored in a RAM (52) (e.g., see figs. 1,5, and col. 11, line 15-col. 12, lines 29) where the storing of the data

pattern to be matched was in a corresponding one of the plural RAMs (a RAM for each channel) as an address and outputting a portion of the data on an M-bit wide output bus in accordance with the value of the address [the bus comprises the parallel output lines of the data channels transferring result outputs in figure 2].

7. It would have bee obvious to one of ordinary skill in the DP art to combine the teachings of Desai and Oh. Both references were directed to the problems of receiving data and matching data in a data stream (e.g., see col.2, lines 33-62 of Oh; col. 6, lines 1-21 of Desai). One of ordinary skill would have been motivated do incorporate the FIFO for receiving the data stream to aid in synchronizing the data transfers especially when the data link has period of idleness (e.g., see col. 2, lines 33-64).

8. As per claim 2, Desai taught the processor for comparing the preset reference pattern with a current data pattern including searching for the data within a data stream (e.g., see fig. 7 and col. 6, lines 1-21). Therefore since individual characters would have been searched and compared and the data to be compared would have to been stored for comparison then one of ordinary skill would have been motivated to incorporate a shift and combinatory logic and a register (e.g., see col. 6, lines 1-21).

9. As per claim 3,14 Desai taught having channelization functionality including an input channel register and a flip-flop array operating a C times slower thatn the first rate for pattern matching(e.g., see col. 5, line 60-col. 6, line 21). Gregg taught instead of flip-flops using RAMs (e.g., see figs. 1,5, and col. 11, line 15-col. 12, lines 29).

10. As per claim 4, Oh, the processor includes means to update the channel state RAM in response to a state change (e.g., see col. 4, lines 37-65 and col. 13, lines 39-51)[update control flags].

11. As per claim 7,9,11, Desai taught a system that detected a data patterns of known length less than a length of the input stream (e.g., see col. 5, line 33-col. 6, line 21). As to the arbitrary length of the data Oh taught a detecting patterns of various lengths (e.g., see col. 3, lines 18-67) by chaining together comparator engines (e.g., see col. 4, lines 7-65).

12. Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Desai (patent No. 6,288,656) in view of Oh etal. (patent No. 6,959,297).

13. Desai taught the invention substantially as claimed including a data processing ("DP") system comprising (as per claims 15,16):

A) A flip-flop (704) for receiving a n bit wide stream(RXD1,RXD2 serial data)(e.g., see fig. 7 and col. 5, lines 33-59) and a corresponding first clock signal at a first rate(recovered clock)(e.g., see fig. 7), and outputting a data stream as a W times N-bit wide data stream and a corresponding stream and a corresponding second clock signal at a second rate divided by W(e.g., see col. 5, lines 33-65);

B) A bus splitter for splitting the W times N-bit wide data stream into W data streams of width N(e.g. se col. 5, lines 33-65)[the data stream is divided or split into data streams send over plural parallel channels];

C) A plurality (W) of flip-flops (712), each flop-flop for storing data obtained by processing the pattern and for receiving a respective one of the data streams of width N

as an address and the second clock signal as a clock, and each flip-flop being operable to output a portion of the data on an M-bit wide output bus[bus comprises the output lines of the flips 712 for the channels e.g. see fig.7);

D) A processor (714) for receiving the portions of data on each M-bit wide output bus as data and the second clock signal as a clock, and being operable to determine whether the pattern is in the data stream in dependence upon the received portions of data and the received clock, and for outputting a pattern match signal indicating detection of the pattern in the data stream(e.g., see fig. 7 and col. 6, lines 3-21) .

14. Desai did not expressly detail that the data pattern after processing was stored in a RAM. Oh however taught the data pattern after processing (input processing in element 22 for putting the data in the form for comparison to be stored in a RAM (52) (e.g., see figs. 1,5, and co. 11, lines 15-col. 12, lines 29) where the storing of the data pattern to be matched was in a corresponding one of the plural RAMs (a RAM for each channel) as an address and outputting a portion of the data on an M-bit wide output bus in accordance with the value of the address [the bus comprises the parallel output lines of the data channels transferring result outputs in figure 2].

15. It would have bee obvious to one of ordinary skill in the DP art to combine the teachings of Desai and Oh. Both references were directed to the problems of receiving data and matching data in a stream the data(e.g., see col.2, lines33-62 of Oh; col. 6, lines 1-21 of Desai). One of ordinary skill would have been motivated do incorporate the FIFO for receiving the data stream to aid in synchronizing the data transfers especially when the data link has period of idleness (e.g., see col. 2, lines 33-64).

16. Desai also taught redirecting either the contents of the processor's register or the contents of the channel state RAM to the processor(e.g., see fig.2; and switching the processor in depending on the received data (e.g., see fig.4 and col. 7, line 67-col. 8, line 21).

17. As per claim 16, Also Oh taught an extendable number of RAMs and means for processing data patterns for a varying amount of data. Therefore, it would have been obvious to one of ordinary skill that the use of plural RAM in parallel provided for the scalability of the system (e.g., see col. 8, lines 22-46)

18.

19. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Heddes. (patent No. 5,450,351).

20. Heddes taught the invention as claimed including data processing ("DP") system comprising:

21. A processor (CAM) for use in a pattern matching engine (e.g., see fig. 2 and col. 5, lines 36-64), the processor having logic means for receiving outputs from the pattern matching RAMS (e.g,. see fig. 2 and col. 6,lines 30-39); a register (e.g,., see fig. 2 and an AND gate for combining the outputs of matching pattern RAMs e.g., see fig. 2) and to output and incation of a matching pattern (e.g., see col. 6, lines 5-39).

22. Heddes did not expressly detail that the logic means was combinatory however since the operation of the logic unit performed a simple operation readily provided in a simple and efficient manner by providing combinatory logic for the clearing of bits one

of ordinary skill would have been motivated to implement the logic unit as using combinatory logic (e.g., see fig. 2 and col. 6,lines 30-39).

Allowable Subject Matter

23. Claims 5,6,8,10 are allowed.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Pitot (patent No. 5,375,142) disclosed a system for detecting and checking template of digital messages (e.g. see abstract and fig. 6).

Henson (patent No. 6,158,014) disclosed a system for automatic detection of 8B/10B data rates (e.g., see abstract) and fig.1).

Potluri (patent No. 6,792,003) disclosed a system for transporting and aligning data across multiple serial data streams (e.g., see abstract).

Freeman (patent No. 4,550,436) disclosed a system for parallel text matching (e.g., see abstract and fig. 4).

Baggenstoss (patent No. 6,535,641) disclosed a class specific classifier (e.g., see abstract).

Lo (patent No. 6,260,167) disclosed an apparatus for deterministic receiver testing (e.g., see abstract and figs. 2,3).

Castellano (patent No. 5,065,396) disclosed an inverse multiplexer and demultiplixer techniques (e.g., see abstract).

Schneider (patent No. 6,201,829) disclosed a serial/parallel transceiver with pattern generator (e.g. see abstract).

Cheng (patent No. 5,525,982) disclosed a system for character string pattern matching (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ERIC COLEMAN
PRIMARY EXAMINER